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Alumina tunnel contact based lateral spin-Field effect transistor

Neetu Gyanchandani^a, Prashant Maheshwary ^b, Kailash Nemade ^{c,*}

^a *JD College of Engineering and Management, Nagpur 441501, India*

^b *Dean (Science and Technology), RTM Nagpur University, Nagpur 440033, India*

^c *Department of Physics, Indira Mahavidyalaya, Kalamb 445401, India*

1. Introduction

For the fabrication of spintronics devices, electrical spin injection and its detection have extraordinary importance [\[1\].](#page-5-0) Recently, few reports have explored that the insertion of tunnel barrier between ferromagnet and semiconducting channel increases the spin injection efficiency of electrode [\[2](#page-5-0)–4].

In case of spin-Field Effect Transistor (s-FET) the important thing is that spin–orbit coupling must be large enough for the transfer of spin and small enough to maintain spin relaxation between source and drain. In s-FET, transistor action can be achieved by two approaches, (i) first is the electrical control of the spin injection process [\[5\]](#page-5-0) and (ii) second is the spin transport efficiency along the channel [\[6\].](#page-5-0)

The major challenge in the realization of s-FET are,

- 1. Efficient spin injection from ferromagnetic source electrode into semiconductor channel.
- 2. Transfer of spin-polarized signal without changing spin through semiconductor channel.
- 3. Detection of spin-polarized signal by ferromagnetic drain electrode.

To resolve these challenges, sufficient knowledge of charge transfer process from ferromagnetic materials to semiconductor is needed. It is well known fact that ferromagnetic materials comprise an excess of electrons having one sided spin, which gives the magnetization direction.

By simply applying the potential difference to FM material, it is not possible to inject quality spin-polarized signal into semiconductor. This difficulty arises due to the huge difference in conductivity of FM material and semiconductor which is also known as conductivity mismatch. To overcome the conductivity mismatch problems, many reports in literature suggest that the insertion of thin layer of insulator between FM and semiconductor enables the spin-dependent tunnel resistance [\[7](#page-5-0)–9]. This results in efficient spin injection into the semiconductor.

In the literature, few reports support to the fabrication device with tunnel contact for efficient spin injection and detection. Erve et al demonstrated graphene as tunnel barrier to resolve the conductivity mismatch problem. Study of Hanle model, this study shows that spin lifetime does not depend on the tunnel barrier material. The main accomplishment of this work is using graphene as tunnel contact stopping metal ion diffusion from the FM electrode [\[10\]](#page-5-0). Schmidt et al suggested that in the diffusive transport region strictly use small polarization current from FM to 2DEG, which results in long spin-flip length [\[11\]](#page-5-0). Cubukcu et al reported significant spin transport in graphenebased lateral spin valves using FM contacts. This study shows that insertion of alumina as tunnel barrier improves spin transfer efficiency by many folds [\[12\].](#page-5-0)

Min et al reported that spin injection from ferromagnet to silicon characteristics using $A₂O₃$ as tunnel contacts. This study concluded that thickness of tunnel contact that is Al_2O_3 and doping concentration of

* Corresponding author. *E-mail address:* krnemade@gmail.com (K. Nemade).

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Fig. 1. Typical structure of spin valve with Co-Graphene nanosheets based FM electrodes separated bytunnel contacts (TC). Dotted red color line indicates active region of device. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

Fig. 2. (a) Schematics of MDD Type silicon based laterals-FET with tunnel contact and (b) Scanning electron micrograph of MDD Type s-FET.

Fig. 3. SEM image of Co-Graphene nanosheets with elemental X-ray mapping of elements (inset).

silicon plays a very crucial role [\[13\]](#page-5-0). Dankert et al validated the production of large spin polarizations in *n*-type and p-type oxidized silicon as a tunnel barrier. In this paper, author explained the role of Schottky

Fig. 4. XRD pattern of (a) alumina, (b) MgO and (c) Co loaded Graphene nanosheets.

barrier in the process of spin injection and detection. Study concluded that width of the Schottky barrier resulted in nondegenerate silicon, which produces an anomalous sign change of spin signal [\[14\].](#page-5-0)Svintsov et al reported the tunnel field effect transistors based on graphene channels. The proposed transistor shows that tunnel gap in the channel operated by gate, which shows ON and OFF state current in semiconductor channels [\[15\]](#page-5-0).

Motivated by the above findings, this paper modified Datta and Das Type silicon based lateral spin-Field Effect Transistor (MDD Type s-FET) is presented with tunnel contact that enhances the spin injection ability of Co-Graphene nanosheets based ferromagnetic electrode (FM). The main accomplishment of present work is that both the key requirements of good s-FET that is non-linear/non-rectifying I–V characteristic and large MR value satisfied by the fabricated device. In spin-transistor technology, high value of MR is an indispensable requirement [\[16\].](#page-5-0) In this work, *n*-type silicon was used as a channel which can control on MR through gate voltage. This is the beauty of present work that MR can be tunable using gate voltage, which enables the switching action in s-FET.

2. Experimentation

2.1. Materials preparation and characterization

In the present study, cobalt anchored graphene nanosheets (Co-Graphene nanoshhets) were prepared by ex-situ approach. In the process of preparation of nanosheets the graphene was used as previously reported method [\[17\].](#page-5-0) To prepare the Co-Graphene nanoshhets, 15 g of graphene sheets were dissolved in 100 ml of acetic acid under constant magnetic stirring for 15 min.

Then solution was subjected to probe-sonication for 30 min. simultaneously, the separate solution of 0.5 g of $Co(NO₃)₃$ was prepared with 20 ml of acetic acid. The second solution of $Co(NO₃)₃$ was added in graphene solution under magnetic stirring at room temperature for 60 min. Lastly, the solution was filtered and washed two times by deionized water. So obtained final product is dried at 100 ◦C in oven. Next, the dried product was kept for heating from 100 to 500 ◦C with an interval of 100 ◦C for 60 min. Then the sample was permitted to cool at 400, 300, 200 and 100 ◦C each for 60 min.

Fig. 5. (a) Non-linear current–voltage curve of Co-Graphene/Alumina/Co-Graphene junction indicating alumina works like a tunnel contact in charge transport. Inset shows general schematic of Co-Graphene/Alumina/Co-Graphene junction. (b) Negative magnetoresistance of Co-Graphene/Alumina/Co-Graphene junction.

Fig. 6. (a) Non-linear current–voltage curve of Co-Graphene/MgO/Co-Graphene junction indicating MgO works like a tunnel contact in charge transport. Inset shows general schematic of Co-Graphene/MgO/Co-Graphene junction. (b) Negative magnetoresistance of Co-Graphene/MgO/Co-Graphene junction.

The X-ray diffraction (XRD) (Rigaku Miniflex-XRD; Wavelength $=$ 1.5406 Å) technique was employed to study structural properties of prepared sample. To analyze the morphology of sample was subjected to field emission scanning electron microscopy on SEM instrument, Model: ZEISS SIGMA. Elemental analysis was completed using an energy dispersive X-ray analysis instrument (Model: EAG AN461).

2.2. Device fabrication and measurements

In this fabrication process, the Co-Graphene/Alumina/Co-Graphene junction and Co-graphene/MgO/Co-Graphene junction were prepared on Si/SiO2 substrate by e-beam evaporation technique. The Co-Graphene nanosheets were used as top and bottom ferromagnetic electrode with thickness of 50 nm by sandwiching the tunnel contacts (in the present work Al_2O_3 and MgO) having thickness of the order of 5 nm. [Fig. 1](#page-1-0) depicts the schematics of complete spin valve device.

To fabricate the modified Datta and Das Type silicon based lateralspin field effect transistor (MDD Type s-FET), all necessary components like heavily doped *n*-type silicon wafer and insulator were procured from India-Mart. The *n*-type silicon wafer used for MDD Type s-FET fabrication have thickness of the order of 500 μm.The details of *n*type silicon waferare resistivity = 10 Ω .m, conductivity = 0.1 S/m, dopant concentration = 4.48 \times $10^6 {\rm m}^{-3}$ and mobility = $0.1351 \text{m}^2 \text{V}^{-1} \text{s}^{-1}$. Firstly, the *n*-type silicon wafer was cleaned to remove the grease, adsorbed water molecule and air borne dust using milddetergent solution (Labolene) and then with distilled water. After cleaning step, using atomic layer deposition technique the two layers of alumina with separation of ~ 0.8 µm was transferred on *n*-type silicon wafer having thickness \sim 5 nm. The alumina was transferred on *n*-type silicon wafer, to resolve the issue of conductivity mismatch between ferromagnetic electrode and semiconductor.

In deposition process, the substrate temperature was maintained at 120 ◦C. The remaining area of substrate was masked with Kapton tape (as it withstands temperatures up to 260 ◦C). Subsequent to this step, Co-Graphene nanosheets based ferromagnetic (FM) electrodes were also deposited on both alumina tunnel contacts. After removal of masking tape, the area between the channel of FM electrodes was coated with polyvinyl acetate using spin-coating technique. The aluminum of thickness 5 nm was transferred as gate on the top of insulating layer of polyvinyl acetate.

As fabricated MDD Type s-FET has channel length of the order of \sim 1.8 μm and channel width \sim 2.3 μm. [Fig. 2](#page-1-0) (a) shows the schematic drawing of MDD Type silicon based laterals-FET with tunnel contact and [Fig. 2\(](#page-1-0)b) shows the scanning electron micrograph of MDD Type silicon based laterals-FET with alumina as tunnel contact and all components of device displayed on SEM image with circuitry arrangement. In the fabrication of MDD Type s-FET with MgO as tunnel barrier, the same process was adopted.

The transport measurements of MDD Type s-FETs with tunnel contact alumina and MgO tested on Physical Properties Measurements

Fig. 7. Gate controlled magnetoresistance in MDD Type silicon based laterals-FET with alumina as tunnel contact at (a) − 0.5 V, (b) − 0.25 V, (c) 0 V, (d) 0.25 V, (e) 0.5 V and (f) 0.75 V.

System (PPMS) made by Quantum Design. The current–voltage curves of both junctions Co-Graphene/Alumina/Co-Graphene junction and Cographene/MgO/Co-Graphene junction were recorded to study the tunneling behavior of junction. The performance of both MDD Type s-FETs with tunnel contact was analyzed by measuring the magnetoresistance (MR) as a function of magnetic field. Similarly, the switching action in MDD Type s-FETs with tunnel contact alumina was revealed in the form of change in amplitude of MR (ΔR_{NL}). MR curves were recorded at 298 K for different values of gate voltages. Magnetoresistance (MR) is defined as, $MR\%=[(Rap-Rp)/Rp] \times 100$, where Rap is magnetization vectors of two electrodes are antiparallel and Rp is the magnetization vectors of two electrodes are parallel.

3. Results and discussion

The surface morphology of Co loaded graphene nanosheets prepared by ex-situ approach was investigated. The SEM image of Co loaded graphene nanosheets with elemental X-ray mapping of cobalt (inset) is shown in [Fig. 3.](#page-1-0) SEM image shows smooth and flat surface with islands of cobalt nanocrystals. The temperature conditioning of Co loaded graphene nanosheets between 100 and 500 ◦C, results in diffusion of Co and O atom [\[18\]](#page-5-0). This diffusion with limited number of crystal seeds available on graphene surface results in the formation of islands. Hence, the SEM image of Co loaded graphene nanosheets have coarse surface due to the presence of islands on graphene. Inset image shows that Co was detected in elemental X-ray mapping.

The quality of the tunnel barrier is very crucial, as the present study

Fig. 8. Variation of resistance change ($ΔR_{NL}$) and spin polarization as a function of gate voltage.

deals with the tunneling at the FM and 2DEG substrate, which depends on the spin of the electrons. To check the structural purity of FM and tunnel contacts, XRD analysis was performed. [Fig. 4](#page-1-0) shows the XRD pattern of (a) alumina, (b) MgO and (c) Co loaded graphene nanosheets, respectively. [Fig. 4](#page-1-0) (a) clearly indicates that alumina used as tunnel contact in MDD Type s-FET have single α-phase $[19]$. The α-alumina phase mostly comprises the characteristics peaks at 2θ angle of 25.5, 35.1, 37.7, 43.3, 52.5, 57.4, 61.2, 66.4 and 68.1 result of miller indices (d_{012}) , (d_{104}) , (d_{110}) , (d_{113}) , (d_{024}) , (d_{116}) , (d_{018}) , (d_{214}) and (d_{300}) , respectively. This data is in good agreement with JCPDS file no. 88–0826 and indicates the rhombohedral structure [\[20](#page-5-0)–21]. The sharp peaks of XRD pattern shows the large grain sizes and well-defined longrange order of alumina. Similarly, the sharp peak indicates the diminishment of the powdery alumina contains [\[22\]](#page-5-0). [Fig. 4\(](#page-1-0)b) shows the XRD pattern of MgO. The pattern exhibits characteristics peaks of MgO at 2θ values of 36.94◦, 42.90◦ and 62.30◦ corresponding to miller indices (d_{111}) , (d_{200}) and (d_{220}) . The XRD data have good agreement with JCPDS card no. 78–0430 [\[23](#page-5-0)–24]. The XRD of MgO comprises the sharp peaks indicates the larger grain size of MgO crystals. [Fig. 4](#page-1-0) (c) shows the XRD pattern of Co-Graphene nanosheets. XRD pattern comprises the signature peaks of graphene at 2θ values 26.3 and 44.2◦ corresponding to miller indices (d_{002}) and (d_{100}). No separate peak for Co appears in XRD pattern indicating that face-to-face stacking is not disturbed due to the introduction of Co in graphene sheets [\[25\]](#page-5-0). The potential reasons for the absence of prominent peaks of Co is that,

- (i) There are lower proportions of Co in the sample. We add 0.5 g of $Co(NO₃)₃$ in 15 g of graphene,
- (ii) The less intensity peaks cannot be observed in the pattern if the other compound is highly crystalline possess high intense XRD peaks. In our case, we add $Co(NO₃)₃$ (by dissolving in 20 ml of acetic acid.) as source of Co.

These are two main and basic reasons for missing peaks in XRD. Therefore, we employ the elemental X-ray mapping technique for the conformation of Co.

To improve the performance of MDD Type s-FET two different types of tunnel contact namely alumina and MgO were used. Some recent reports revealed that the use of tunnel contact improves the spin injection efficiency of FM and resolve the issue of conductivity mismatch between FM and semiconductor [\[26\].](#page-5-0)

[Fig. 5](#page-2-0) (a) shows the non-linear I-V curve of Co-Graphene/Alumina/ Co-Graphene junction at 298 K indicating that alumina works like a tunnel contact in charge transport process. Inset of figure shows general schematic of Co-Graphene/Alumina/Co-Graphene junction. [Fig. 5](#page-2-0) (b) shows the MR of Co-Graphene/Alumina/Co-Graphene junction. The observed MR has negative magnitude which indicates the change in

polarity. This negative value of MR clears that alumina as tunnel contact works like filter, which filters the majority spins of the FM electrode [\[27\]](#page-5-0). [Fig. 6](#page-2-0) (a) shows the non-linear I-V curve for Co-Graphene/MgO/ Co-Graphene junction at 298 K, also shows tunneling behavior of MgO tunnel contact. Inset shows the schematic of Co Graphene/Alumina/Co-Graphene junction. In this case, MR shows negative magnitude, which indicates that MgO layer also displays the characteristics of filtering the spin. The comparison of both devices shows that insertion of alumina layer between FM electrode results in significant enhancement of MR compared to MgO layer. Besides this IV characteristics of both layers indicate that it works like a tunnel barrier and filter for spin. In the comparison of both tunnel contacts that is alumina and MgO, it is clearly observed that MR value using alumina as tunnel contact is higher than the MgO. Hence, subsequent study of MDD Type s-FET is confined to alumina as tunnel contact.

3.1. Electrical gate-tuning of the MR

In this subsection, it is demonstrated that the MR can be controlled using gate voltage. In this process, gate voltage is used to diffuse the direction of spin signal. This blocking of spins in *n*-type silicon channel gives additional control on MR value of device. Electric field via gate can influence the MR by routes [\[28,29\],](#page-5-0)

- 1. Electric field can change the spin accumulation density of silicon channel.
- 2. It has ability of spin-to charge conversion.

Mechanism behind MR for gate voltage is that spin gathering close to FM contact is responsible for a spin-dependent voltage. This can be measured by using Silsbee–Johnson spin charge coupling [\[30\].](#page-5-0)

[Fig. 7](#page-3-0) (a-f) shows the gate-controlled MR in MDD Typesilicon based lateral s-FET with alumina as tunnel contact for different value of gate voltage from − 0.5 V to 0.75 V at room temperature. The highest value of MR associated with gate voltage is -0.5 V [\(Fig. 7-](#page-3-0)a), whereas it reduces almost in linear manner up to 0.5 V ([Fig. 7-](#page-3-0)e). For the gate voltage 0.75 V ([Fig. 7-](#page-3-0)f), the MR vanishes. This dependence of MR on gate voltage enables the devices for switching application.

Fig. 8. depicts the variation of resistance change (ΔR_{NL}) and spin polarization as a function of gate voltage 298 K. The values of spin polarization estimated for negative values of MR using (Eq.1),

$$
MR = \frac{2P_1P_2e^{\frac{-d}{\lambda_s}}}{1 - P_1P_2e^{\frac{-d}{\lambda_s}}} \tag{1}
$$

where d is the length of the trajectories of the electrons. For the sufficiently high separation of electrodes, the value of surviving probability factor[$exp(-d/\lambda_s)$] nearly equal to 1.

Both parameters, ΔR_{NL} and spin polarization have cross dependence as a function of gate voltage. The ΔR_{NL} curve shows the MDD Type s-FET exhibits the switching characteristics. The magnitude of the ΔR_{NL} decreases in a monotonic and nonlinear fashion with increasing gate voltage. Below $Vg = 0 V$, MR has highest magnitude whereas it reduces linearly and vanishes at 0.75 V.

4. Conclusions

In summary, MDD Type silicon based laterals-FET is studied in order to improve the spin injection and to resolve the conductivity mismatch between FM and 2DEG.Main outcome of the present work is that s-FET with alumina as tunnel contact exhibits the non-rectifying IV characteristic and considerable MR, which is an indispensable requirement for spintronics device fabrication. Similarly, the key accomplishment of this report is MR can be tunable using gate voltage, which enables the switching action in s-FET. The obtained results are very motivating for future graphene-based spintronic devices.

5. Data availability

The raw/processed data required to reproduce these findings cannot be shared at this time as the data also forms part of an ongoing study.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

No data was used for the research described in the article.

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